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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/627,165	07/24/2003	Thomas Laursen	004.0033	2527

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EXAMINER	
SMITH, NICHOLAS A	
ART UNIT	**PAPER NUMBER**
1742	

DATE MAILED: 06/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/627,165	LAURSEN ET AL.	
	Examiner	Art Unit	
	Nicholas A. Smith	1742	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/24/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

Claims 1-21 remain for examination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-3, 6-11, 13-14 and 16-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Chen et al. (US Patent 6,811,680).

In regards to claim 1, Chen et al. anticipates a method for planarizing a semiconductor wafer (col.1, lines 17-19) with an insulating layer comprising a field region and a plurality of features (col. 1, lines 31-34), comprising the steps of forming a barrier layer over at least the field region (col. 2, lines 21-23), electrodepositing a copper layer with a substantially planar surface overlying the barrier layer (col. 2, lines 12-16)

and filling in the features of the insulating layer (col. 1, lines 23-26), and also polishing a layer comprising copper and the barrier layer on a single polishing pad to remove this layer comprising copper and the barrier layer from the field region (col. 1, lines 55-67 and col. 2, lines 1-4).

In regards to claim 2, Chen et al. anticipates a method comprising chemical mechanical planarizing on a single soft polishing pad (col. 25, lines 55-60).

In regards to claim 3, Chen et al. anticipates chemical mechanical planarizing on a polishing pad. While Chen et al. does not specifically mention the Shore D hardness of the polishing pads used, Chen et al. does mention the use of Politex series pads from Rodel, Inc. (col. 11, lines 13-18) just as the instant invention uses Politex pads from Rodel, Inc. (p. 8, specification). It is the examiner's position that the Politex pads in Chen et al. are inherently having the same hardness less than about 0.4 on the Shore D hardness scale as claimed because the same products should have the same properties. See MPEP 2112.01 I.

In regards to claim 6, Chen et al. anticipates a method comprising the steps of cleaning and buffing the field region following the step of polishing (col. 25, lines 53-67 and col. 26, lines 1-12).

In regards to claim 7, Chen et al. anticipates forming a barrier layer over the field region comprising a low-k dielectric material insulating layer (col. 2, lines 57-60).

In regards to claim 8, Chen et al. anticipates polishing the insulating layer on the single polishing pad to planarize the field region (col. 22, lines 4-7).

In regards to claim 9, Chen et al. anticipates electrodepositing on a first platen of a multi-platen apparatus and polishing on a second platen of the multi-platen apparatus (col. 5, lines 38-43).

In regards to claim 10, Chen et al. anticipates cleaning the polished copper layer on a buff polishing station on a third platen of the multi-platen apparatus (col. 25, lines 53-64).

In regards to claim 11, Chen et al. anticipates forming a seed layer comprising copper overlying the barrier layer (col. 15, lines 29-35) and electrodepositing over the seed layer a second layer comprising copper having thickness less than about 300 nm over the field region (col. 23, lines 18-21).

In regards to claim 13, Chen et al. anticipates a method for planarizing a semiconductor wafer (col.1, lines 17-19) with an insulating layer of low-k dielectric material (col. 2, lines 57-60) comprising a field region and a plurality of features (col. 1, lines 31-34), comprising the steps of forming a barrier layer over the insulating layer (col. 2, lines 21-23), forming a seed layer comprising copper overlying the barrier layer (col. 15, lines 29-35), electrodepositing a copper layer with a substantially planar surface overlying the seed layer that is over the barrier layer (col. 2, lines 12-16) and filling in the features of the insulating layer (col. 1, lines 23-26), and also chemical mechanical polishing a layer comprising copper and the barrier layer on a single polishing platen to remove this layer comprising copper and the barrier layer from the field region (col. 1, lines 55-67 and col. 2, lines 1-4).

In regards to claim 14, Chen et al. anticipates the step of chemical mechanical polishing comprising the step of electrochemical mechanical polishing (col. 4, lines 58-65).

In regards to claim 16, Chen et al. anticipates a method comprising chemical mechanical polishing on a single soft polishing pad on the single platen (col. 25, lines 55-60).

In regards to claim 17, Chen et al. anticipates a method for planarizing a work piece (col.1, lines 17-19) comprising a field region and a plurality of features (col. 1, lines 31-34), comprising the steps of forming a barrier layer over field region and extending into the features (col. 2, lines 21-23), electrodepositing a metal layer with a substantially planar surface overlying the barrier layer (col. 2, lines 12-16) and filling in the features (col. 1, lines 23-26), and also polishing a metal layer and the barrier layer on a single polishing pad to remove this metal layer and the barrier layer from the field region (col. 1, lines 55-67 and col. 2, lines 1-4).

In regards to claim 18, Chen et al. anticipates electrodepositing on a first platen of a multi-platen apparatus and polishing on a second platen of the multi-platen electrochemical mechanical planarization apparatus (col. 5, lines 38-43).

In regards to claim 19, Chen et al. anticipates electrodepositing a metal layer at a first platen of the multi-platen apparatus (col. 5, lines 38-43), robotically moving the work piece to a second platen of the multi-platen apparatus (col. 5, lines 50-52) and polishing the metal layer and the barrier layer at the second platen (col. 5, lines 38-43).

In regards to claim 20, Chen et al. anticipates a work piece mounted on a work piece carrier (col. 12, lines 36-39), comprising aligning the work piece carrier with respect to a first and a second platen of the multi-platen apparatus (col. 12, lines 56-67 and col. 13, lines 1-3), electrodepositing a metal layer at the first platen (col. 5, lines 38-43) and polishing the metal layer and the barrier layer at the second platen (col. 5, lines 38-43).

In regards to claim 21, Chen et al. anticipates polishing a metal layer and a barrier layer on a single polishing pad at a pressure between the work piece and the polishing pad of less than about 2.5 psi (col. 25, lines 55-60). In regards to the feature of a "polishing pad having hardness of less than about 0.4 on the Shore D hardness scale," same reasoning applies as above.

Claim Rejections - 35 USC § 103

Claims 4 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. in view of Sinha et al. (US Patent 6,551,935).

In regards to claims 4 and 12, Chen et al. teaches all the features of claims 2 and 1, respectively.

However, Chen et al. does not teach the method of chemical mechanical planarizing in the presence of polishing slurry having a copper-barrier layer selectivity of substantially 1:1.

Sinha et al. teaches the method of chemical mechanical planarizing in the presence of polishing slurry having a copper-barrier layer selectivity of substantially 1:1 (abstract). It would have been obvious to one of ordinary skill in the art at the time of

invention to apply Sinha et al.'s slurry in Chen et al.'s chemical mechanical planarizing method because have a 1:1 selectivity would keep gaps from forming in locations where the barrier material should be located and consequently keep the copper layer from undesirably diffusing into unprotected regions of the substrate (Sinha et al., col. 2, lines 25-52).

Claims 5 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. in view of Sinha et al. and further in view of Lee et al. (US Patent 6,919,276).

In regards to claims 5 and 15, Chen et al. teaches all the features of independent claims 2 and 13, respectively. Sinha et al. teaches the use of a substantially 1:1 copper to barrier layer selectivity slurry as above.

However, Chen et al. in view of Sinha et al. does not teach the use of a first slurry having a selectivity of copper to barrier layer greater than 1:1 to remove the first portion of the copper layer.

Lee et al. does teach the use of multiple slurries, one slurry specified for the first portion of the copper layer. Each slurry has its own desired selectivity and removal rate (col. 1, lines 56-67 and col. 2, lines 1-2). As the first slurry is directed towards copper removal, one would choose this first slurry to be selective towards copper, i.e., a selectivity of copper to barrier layer greater than 1:1 to remove the first portion of the copper layer. It would have been obvious to one of ordinary skill in the art at the time of invention to apply Lee et al.'s slurry method to Chen et al.'s method in view of Sinha et al. because using a slurry having a higher selectivity's for material removal of the

copper layer with respect to the barrier layer results in improving planarity, reducing erosion (Lee et al., col. 2, lines 34-37) and to minimize the required polishing time for relatively thick overlayers of excess copper (Lee et al., col. 1, lines 62-65).

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Tsai et al. (US 2003/0013387) describes chemical mechanical planarzing with respect to barrier layer removal.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nicholas A. Smith whose telephone number is (571)-272-8760. The examiner can normally be reached on 8:30 AM to 5:00 PM, Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Roy King can be reached on (571)-272-1244. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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